ECE 4240 – Microprocessor Interfacing

Fall 2021

IMPORTANT NOTICE – Mandatory Requirement to Report

This course will be conducted using remote instruction. Students who are accessing the course from outside of Canada or the USA must notify the instructor and indicate in which country they are located. Access to software may be restricted from some countries and failure to comply with these restrictions may result in criminal prosecution.

Course Objectives

The course presents real-time wired and wireless interfacing of microcontrollers, microprocessors, and microcomputers to the external world, including interfacing of I/O devices with minimum hardware and software, data acquisition, and some aspects of data communications, transmission and logging with embedded systems.

Course Content

The following topics will be covered:

• Overview of computing, architectures, processors, and technologies
• Bus architectures
• Digital input and output (I/O) architectures and organization
• Digital-to-analog (D/A) and A/D signal conversions and converters
• Interfacing aspects in data communications related to real time
• Updates on new concepts, technologies, protocols, and software
• Demos: Examples of bus architectures, modules, systems, and new devices.
• Updates on new computer concepts, technologies, protocols, and software.

Textbook


Other Resources


Other Supplementary Material
- Books and Data Sheets
  - The library has many other books covering different aspects of microprocessor and microcomputer interfacing. Laboratory write-ups provide detailed description of the devices used. Data sheets should also be consulted for specific parameters of the devices. As usual, information on current developments in interfacing is published in numerous technical magazines and journals, including:
  - Magazines (examples)
  - Journals (examples)

Learning Outcomes
1. Describe the role of the essential elements of interfacing in real-time systems.
2. Analyze the best techniques for synchronization in digital systems.
3. Analyze and design the best techniques for analog-to-digital conversion (DAC).
4. Analyze and design the best techniques for digital-to-analog conversion (ADC).
5. Analyze and design modern data transmission systems in the presence of noise.
6. Analyze and design simple error detection and correction systems.
7. Solve open-ended problems of data transmitting data in the presence of noise.

Expected Competency Levels

<table>
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<tr>
<th>Outcome</th>
<th>KB</th>
<th>PA</th>
<th>IN</th>
<th>DE</th>
<th>ET</th>
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Evaluation
The final course grade is determined by the student’s performance on assignments, in laboratories, in two midterm tests, and on the final examination. Students must complete all the laboratories in order to be eligible to receive a passing grade.

<table>
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<th>Component</th>
<th>Value (%)</th>
<th>Method of Feedback</th>
<th>Learning Outcomes Evaluated</th>
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* Method of Feedback: F - Formative (written comments and/or oral discussion), S - summative (numerical grade)
CEAB Graduate Attributes Assessed

IN.3 – Interprets results and reaches appropriate conclusions.

DE.3 – Develops/implements possible solutions to an open-ended design problem, leading to an appropriate recommendation.

Academic Integrity

Students are expected to conduct themselves in accordance with the highest ethical standards of the Profession of Engineering and evince academic integrity in all their pursuits and activities at the university. As such, in accordance with the General Academic Regulations on Academic Integrity, students are reminded that plagiarism or any other form of cheating in examinations, term tests, assignments, projects, or laboratory reports is subject to serious academic penalty (e.g. suspension or expulsion from the faculty or university). A student found guilty of contributing to cheating by another student is also subject to serious academic penalty.

Requirements and Regulations

• Attendance at lectures and laboratories is essential for successful completion of this course. Students must satisfy each evaluation component in the course to receive a final grade.
• It is the responsibility of each student to contact the instructor in a timely manner if he or she is uncertain about his or her standing in the course and about his or her potential for receiving a failing grade. Students should also familiarize themselves with the University’s General Academic Regulations, as well as Section 3 of the Faculty of Engineering Academic Regulations dealing with incomplete term work, deferred examinations, attendance and withdrawal.
• No programmable devices or systems (such as calculators, PDAs, iPods, iPads, cell phones, wireless communication or data storage devices) are allowed in examinations unless approved by the course instructor.
• Students should be aware that they have access to an extensive range of resources and support organizations. These include Academic Resources, Counselling, Advocacy and Accessibility Offices as well as documentation of key University policies e.g. Academic Integrity, Respectful Behaviour, Examinations and related matters.

Copyright Notice

All materials provided in this course are copyright and are provided under the fair dealing provision of the Canadian Copyright Act. This material may not be redistributed in any manner without the express written permission of the relevant copyright holder.

Retention of Student Work

Students are advised that copies of their work submitted in completing course requirements (i.e. assignments, laboratory reports, project reports, test papers, examination papers, etc.) may be retained by the instructor and/or the department for the purpose of student assessment and grading, and to support the ongoing accreditation of each Engineering program. This material shall be handled in accordance with the University’s Intellectual Property Policy and the protection of privacy provisions of The Freedom of Information and Protection of Privacy Act (Manitoba). Students who do not wish to have their work retained must inform the Head of Department, in writing, at their earliest opportunity.