Course Description
This course introduces advanced topics in computer architecture and organization. Topics include instruction set architecture, performance measures, pipeline processor design, data and instruction cache, data dependencies, branch prediction and penalties, and multiprocessor system design. As well, this course is concerned with an engineering approach to selecting and interconnecting hardware components to create computers that meet functional, performance and cost goals. The course covers improvements and refinements to the basic computer designs as taught in undergraduate courses, and is intended to be a successor of same. Therefore, it is crucial that students have a good grasp of basic computer architecture as taught at ECE 3610 or in similar classes elsewhere.

Prerequisites
• ECE 3610 Micro-Processor Systems

Course Content
The following topics will be covered:
• Instruction Set Architecture
  • Components, Instruction Lengths and Formats, Very Long Instruction Word, ARM, MIPS
• Performance – Meaning and Metrics
  • Computer Metrics – efficiency, throughput, latency, etc.
  • Moore’s Law, Amdahl’s Law
  • MIPS, MFLOPS, SPEC, and benchmarks
• Processor Control
  • Hardwired vs. Microprogram
• Pipelining
  • Data and Branch Hazards, Stalls, and Branch Penalty
  • Static and Dynamic Branch Prediction and Speculative Execution
• Cache Memory Systems
  • (Fully Associative, Direct Mapped, Set-Associative, and Pseudo-Associative) Cache Structure
  • Performance
  • Considerations of Cache Design
• Input/Output
  • Advanced Interrupt Strategies
• Computer Bus
  • History, review, and evolutionary perspectives of computer buses: VME, NuBus, PCI, PCIe, Firewire, USB
  • Bus Arbitration
• Parallel Processing and Multicore
  • Superscalar, multithreading, parallel processing, multi-core CPUs
  • In-order and out-of-order instruction execution
  • Multiple-instruction instruction word
  • Superscalar pipelining
  • Compiler and hardware instruction level parallelism
  • Cache Coherency
  • Multiprocessor Topologies
    • Partial and Fully Connected (Crossbar, Butterfly, Cluster, Multiprocessor Interconnection Networks)
Lab Content
The following topics may be covered in the labs:

- Incremental design and development of a soft basic 8-bit microprocessor, using Verilog and Altera’s DE-2 board. The incremental steps will be:
  - Non-pipelined micro-programmed computer control unit (CCU).
    - Control signals are accessed through a micro-programmed memory.
  - Non-pipelined hardwired, dynamic logic computer control unit (CCU).
    - Control signals are generated by logic circuits dynamically
  - Five stage single pipeline
  - Five stage dual pipeline
  - Out of order execution
  - Branch predictor
  - Multiple instruction fetch unit
- Several labs on Altera’s NIOS processor.

Accreditation Units
- Mathematics: 0%
- Natural Science: 0%
- Complementary Studies: 0%
- Engineering Science: 75%
- Engineering Design: 25%

Web Page
- http://ece.eng.umanitoba.ca/undergraduate/ECE4580T02

Textbook

Other References

Evaluation Details
The final course grade will be determined from a student’s performance in the projects and on examinations. In order to receive a passing grade in this course:

1. All projects must be completed and a passing grade must be achieved.
2. A passing grade in the final exam must be achieved.

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
<th>Details</th>
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<tbody>
<tr>
<td>Projects: Assignments and Labs</td>
<td>30%</td>
<td>All must be submitted and a passing grade achieved.</td>
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<tr>
<td>Term Test</td>
<td>20%</td>
<td>Thursday, November 6, 2014, 6:00-8:00 PM (location TBA)</td>
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<tr>
<td>Final Examination</td>
<td>50%</td>
<td>TBA</td>
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Instructor
- Prof. K. Ferens. Ph.D., P.Eng.
- Room: E1-544 EITC
- Telephone: (204) 474-8517
- Email: Ken.Ferens@umanitoba.ca
Office Hours
• By appointment.

Teaching Assistant
• TBA

Voluntary Withdrawal Date
• Wednesday, November 12th, 2014.

Requirements/Regulations
• Attendance at lectures and laboratories is essential for successful completion of this course. Students must satisfy each evaluation component in the course to receive a final grade.
• It is the responsibility of each student to contact the instructor in a timely manner if he or she is uncertain about his or her standing in the course and about his or her potential for receiving a failing grade. Students should also familiarize themselves with Sections 4 and 6 of the Regulations dealing with incomplete term work, deferred examinations, attendance and withdrawal.
• No programmable devices or systems (such as calculators, PDAs, iPods, iPads, cell phones, wireless communication or data storage devices) are allowed in examinations unless approved by the course instructor.

Academic Integrity
Students are expected to conduct themselves in accordance with the highest ethical standards of the Profession of Engineering and evince academic integrity in all their pursuits and activities at the university. As such, in accordance with the General Academic Regulations and Requirements of the University of Manitoba, Section 7.1, students are reminded that plagiarism or any other form of cheating in examinations, assignments, laboratory reports or term tests is subject to serious academic penalty (e.g. suspension or expulsion from the faculty or university). A student found guilty of contributing to cheating in examinations or term assignments is also subject to serious academic penalty.

Learning Outcomes
1. Identify advanced topics in computer architecture and organization.
2. Demonstrate the ability to create new macroinstructions by designing new and reusing existing microinstructions.
3. Demonstrate the ability to analyze a given pipelined system and identify potential hazards.
4. Demonstrate the ability to analyze a given problem to determine the appropriate level and size of cache memory to use in a design of an embedded system.

<table>
<thead>
<tr>
<th>Learning Outcome</th>
<th>A1</th>
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**Attributes:**
A1 A knowledge base for engineering
A2 Problem analysis
A3 Investigation
A4 Design
A5 Use of engineering tools
A6 Individual and team work
A7 Communication skills
A8 Professionalism
A9 Impact of engineering on society/environment
A10 Ethics and equity
A11 Economics and project management
A12 Life-long learning

**Competency Levels:**
1 - Knowledge (Able to recall information)
2 - Comprehension (Able to rephrase information)
3 - Application (Able to apply knowledge in a new situation)
4 - Analysis (Able to break problem into its components and establish relationships)
5 - Synthesis (Able to combine separate elements into whole)
6 - Evaluation (Able to judge of the worth of something)

**Student Contact Time (Hrs)**
Lectures: 3 hrs lecture/week × 13 weeks/term = 39 hrs
Laboratories: 3 hrs laboratory × 5 weeks = 15 hrs
Tutorials: 0 hr tutorial × 0 weeks = 0 hrs

**Evaluation**

<table>
<thead>
<tr>
<th>Component</th>
<th>Value (%)</th>
<th>Methods of Feedback *</th>
<th>Learning Outcomes Evaluated</th>
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<tbody>
<tr>
<td>Projects</td>
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<td>F, S</td>
<td>1-7</td>
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<tr>
<td>Mid-Term Test</td>
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<td>F, S</td>
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<tr>
<td>Final Examination</td>
<td>50</td>
<td>S</td>
<td>1-7</td>
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*Methods of Feedback: F - formative (written comments and/or oral discussion), S - summative (number grades)