ECE 4740 – Digital System Implementation

Course Objectives
Implementation methodologies and technologies for digital systems, including application specific integrated circuits (ASICs), system on chip (SoC) and rapid prototyping using Field Programmable Gate Arrays (FPGA). A good understanding of test techniques and improving reliability from a systems perspective is a concomitant objective.

Course Content
The following topics will be covered:
• Integrated circuit overview
• Basic MOS transistor operation
• The CMOS inverter in detail as a building block
• CMOS-VLSI fabrication (minimal)
• Performance issues and basic transmission lines
• Basic circuits (minimal)
• Abstractions for simulation and modelling. (Elmore delay through to static timing analysis.)
• Regular structures (Embedded memory and flash)
• Integrated circuit faults and models
• Design for test (scan based design and built-in self-test.)
• Fault tolerant design

Laboratories
The laboratories will focus on reliability of electronic components, sub-systems and systems, through both hardware and encoding technique simulations. Results will be achieved through building simulation models.

Textbook
On-line notes and presentation materials.

Other Resources
Modelling, Synthesis and Rapid Prototyping with the Verilog HDL, M.D. Ciletti, Prentice Hall, 1999.

Requirements and Regulations
• Attendance at lectures and laboratories is important for successful completion of this course. Students must satisfy each evaluation component in the course to receive a final grade.
• It is the responsibility of each student to contact the instructor in a timely manner if he or she is uncertain about his or her standing in the course and about his or her potential for receiving a failing grade. Students should also familiarize themselves with the University’s General Academic Regulations, as well as Section 3 of the Faculty of Engineering Academic Regulations dealing with incomplete term work, deferred examinations, attendance and withdrawal.
• No programmable devices or systems (such as calculators, PDAs, iPods, iPads, cell phones, wireless communication or data storage devices) are allowed in examinations unless approved by the course instructor.
• Students should be aware that they have access to an extensive range of resources and support organizations. These include Academic Resources, Counselling, Advocacy and Accessibility Offices as well as documentation of key University policies e.g. Academic Integrity, Respectful Behaviour, Examinations and related matters.
Learning Outcomes

1. Interpret and paraphrase the operation of MOS Transistors and the CMOS Inverter.
2. Design simple logic gates in a bottom up fashion.
3. Evaluate system design and design trade-offs as it pertains to chip level systems.
4. Construct reliability simulations of components and systems.

Expected Competency Levels

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<thead>
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<th>Outcome</th>
<th>KB</th>
<th>PA</th>
<th>IN</th>
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<th>PR</th>
<th>IE</th>
<th>EE</th>
<th>EP</th>
<th>LL</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>3</td>
<td>3</td>
<td>3</td>
<td>4</td>
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<td>6</td>
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Evaluation

The final course grade is determined by the student’s performance on assignments, in laboratories, and on examinations. Students must complete a subset of the laboratories in order to be eligible to receive a passing grade.

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<tr>
<th>Component</th>
<th>Value (%)</th>
<th>Method of Feedback</th>
<th>Learning Outcomes Evaluated</th>
</tr>
</thead>
<tbody>
<tr>
<td>Assignments</td>
<td>5</td>
<td>F, S</td>
<td>1, 2</td>
</tr>
<tr>
<td>Laboratories</td>
<td>25</td>
<td>F, S</td>
<td>3, 4</td>
</tr>
<tr>
<td>Term Test</td>
<td>20</td>
<td>F, S</td>
<td>1, 2, 3</td>
</tr>
<tr>
<td>Final Examination</td>
<td>50</td>
<td>S</td>
<td>1, 2, 3</td>
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* Method of Feedback: F - Formative (written comments and/or oral discussion), S - summative (numerical grade)

CEAB Graduate Attributes Assessed

PA.4 – Evaluates a solution to a complex engineering problem.

ET.2 – Evaluates and selects appropriate tools for a given scenario.

Academic Integrity

Students are expected to conduct themselves in accordance with the highest ethical standards of the Profession of Engineering and evince academic integrity in all their pursuits and activities at the university. As such, in accordance with the General Academic Regulations on Academic Integrity, students are reminded that plagiarism or any other form of cheating in examinations, term tests, assignments, projects, or laboratory reports is subject to serious academic penalty (e.g. suspension or expulsion from the faculty or university). A student found guilty of contributing to cheating by another student is also subject to serious academic penalty.

Retention of Student Work

Students are advised that copies of their work submitted in completing course requirements (i.e. assignments, laboratory reports, project reports, test papers, examination papers, etc.) may be retained by the instructor and/or the department for the purpose of student assessment and grading, and to support the ongoing accreditation of each Engineering program. This material shall be handled in accordance with the University’s Intellectual Property Policy and the protection of privacy provisions of The Freedom of Information and Protection of Privacy Act (Manitoba). Students who do not wish to have their work retained must inform the Head of Department, in writing, at their earliest opportunity.