Course Objectives
Implementation methodologies and technologies for digital systems, including very large scale integration (VLSI), application specific integrated circuits (ASICs), system on chip (SoC) and rapid prototyping using Field Programmable Gate Arrays (FPGA).

Prerequisites
ECE 4240 Microprocessor Interfacing

Course Content
The following topics will be covered:
- Integrated circuit overview
- Basic MOS transistor operation
- The CMOS inverter in detail
- CMOS-VLSI fabrication (minimal)
- Performance issues and basic transmission lines
- Basic circuits (minimal)
- Design tools (minimal)
- Alternative CMOS gates (minimal)
- Regular structures (embedded memory and flash)
- Structured design
- Integrated circuit faults and models
- Conventional test
- Design for test (scan based design)
- Fault tolerant design (if time permits)

Accreditation Units
Mathematics: 5%
Natural Science: 0%
Complementary Studies: 5%
Engineering Science: 30%
Engineering Design: 60%

Web Page
https://universityofmanitoba.desire2learn.com/

Textbook (not required)
Course notes available online. Labs information is available online from course webpage on “D2L”.

Other References

*Modelling, Synthesis and Rapid Prototyping with the Verilog HDL*, Michael D. Ciletti, Prentice Hall.
Other references available on course web page.
**Evaluation Details**
The final course grade is determined by the student’s performance on assignments, in laboratories, and on examinations. Students must complete a subset of the laboratories in order to be eligible to receive a passing grade.

**Mid-Term**
In class, date TBA

**Instructor**
Prof. Bob McLeod, Ph.D., P.Eng.
Room: E1-548 EITC
Telephone: (204) 474-8886
Email: mcleod@ee.umanitoba.ca

**Office Hours**
After lectures or by appointment. Students are also welcome to drop by E3-416 between 9:00 AM-5:00 PM any day.

**Teaching Assistants**
TBA

**Voluntary Withdrawal Date**
Wednesday, November 12th, 2014.

**Requirements/Regulations**
- Attendance at lectures and laboratories is useful for successful completion of this course. Students must satisfy each evaluation component in the course to receive a final grade.
- It is the responsibility of each student to contact the instructor *in a timely manner* if he or she is uncertain about his or her standing in the course and about his or her potential for receiving a failing grade. Students should also familiarize themselves with Sections 4 and 6 of the Regulations dealing with incomplete term work, deferred examinations, attendance and withdrawal.
- No programmable devices or systems (such as calculators, PDAs, iPods, iPads, cell phones, wireless communication or data storage devices) are allowed in examinations unless approved by the course instructor.

**Academic Integrity**
Students are expected to conduct themselves in accordance with the highest ethical standards of the Profession of Engineering and evince academic integrity in all their pursuits and activities at the university. As such, in accordance with the General Academic Regulations and Requirements of the University of Manitoba, Section 7.1, students are reminded that plagiarism or any other form of cheating in examinations, assignments, laboratory reports or term tests is subject to serious academic penalty (e.g. suspension or expulsion from the faculty or university). A student found guilty of contributing to cheating in examinations or term assignments is also subject to serious academic penalty.
Learning Outcomes

1. Interpret and paraphrase the operation of MOS Transistors and the CMOS Inverter.
2. Design simple logic gates in a bottom up fashion.
3. Evaluate system design and design trade-offs as it pertains to chip level systems.
4. Construct FPGA designs using Verilog and ModelSim.

Expected Competency Level **

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<th>Learning Outcome</th>
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*Attributes:
A1 A knowledge base for engineering
A2 Problem analysis
A3 Investigation
A4 Design
A5 Use of engineering tools
A6 Individual and team work
A7 Communication skills
A8 Professionalism
A9 Impact of engineering on society/environment
A10 Ethics and equity
A11 Economics and project management
A12 Life-long learning

**Competency Levels:
1 - Knowledge (Able to recall information)
2 - Comprehension (Able to rephrase information)
3 - Application (Able to apply knowledge in a new situation)
4 - Analysis (Able to break problem into its components and establish relationships)
5 - Synthesis (Able to combine separate elements into whole)
6 - Evaluation (Able to judge of the worth of something)

Student Contact Time (Hrs)

Lectures: 3 hrs lecture/week × 13 weeks/term = 39 hrs
Laboratories: 3 hrs laboratory × 5 weeks = 15 hrs
Tutorials: 0 hr tutorial × 0 weeks = 0 hrs

Evaluation

<table>
<thead>
<tr>
<th>Component</th>
<th>Value (%)</th>
<th>Methods of Feedback *</th>
<th>Learning Outcomes Evaluated</th>
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<tr>
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* Methods of Feedback: F - formative (written comments and/or oral discussion), S - summative (number grades)