University of Manitoba | Price Faculty of Engineering
Department of Electrical and Computer Engineering

Course Outline

Instructor

- Prof. Bob McLeod, P.Eng.
  E1–548 EITC
  (204) 474–8886
  Robert.McLeod@umanitoba.ca

Office Hours
- Students may also drop by E3–416 between 9:00AM–5:00PM.

Teaching Assistant
- Debarati Nath
  nathd1@myumanitoba.ca

Contact Hours
- 4 credit hours
- Lectures:
  3 hours x 13 weeks = 39 hours
- Laboratories:
  3 hours x 5 weeks = 15 hours

Prerequisites:
- ECE 4240 Microprocessor Interfacing

Course Website:
https://umanitoba.ca/umlearn

Important Dates

- **Term Test**
  TBD
- **Voluntary Withdrawal Deadline**
  November 23rd, 2020
- **Thanksgiving Day**
  October 12th, 2020
  No classes or examinations
- **Remembrance Day**
  November 11th, 2020
  No classes or examinations
- **Fall Term Break**
  November 9th–13th, 2020
  No classes or examinations

ECE 4740 – Digital System Implementation

Fall 2020

IMPORTANT NOTICE – Mandatory Requirement to Report

This course will be conducted using remote instruction. Students who are accessing the course from outside of Canada or the USA ***must notify the instructor*** and indicate in which country they are located. Access to software may be restricted from some countries and failure to comply with these restrictions may result in criminal prosecution.

Course Objectives

Implementation methodologies and technologies for digital systems, including application specific integrated circuits (ASICs), system on chip (SoC) and rapid prototyping using Field Programmable Gate Arrays (FPGA). A good understanding of test techniques and improving reliability from a systems perspective is a concomitant objective.

Course Content

The following topics will be covered:

- Integrated circuit overview
- Basic MOS transistor operation
- The CMOS inverter in detail as a building block
- CMOS-VLSI fabrication (minimal)
- Performance issues and basic transmission lines
- Basic circuits (minimal)
- Abstractions for simulation and modelling. (Elmore delay through to static timing analysis.)
- Regular structures (Embedded memory and flash)
- Integrated circuit faults and models
- Design for test (scan based design and built-in self-test.)
- Fault tolerant design

Laboratories

The laboratories will focus on reliability of electronic components, sub-systems and systems, through both hardware and encoding technique simulations. Results will be achieved through building simulation models.

Textbook

On-line notes and presentation materials.

Other Resources

Digital Design: A Systems Approach, W.J. Dally, R.C. Harting, Cambridge University Press, 2012.
Modelling, Synthesis and Rapid Prototyping with the Verilog HDL, M.D. Ciletti, Prentice Hall, 1999.
Fundamentals of Digital Logic with Verilog Design, S. Brown and Z. Vranesic, McGraw-Hill 2014.

Academic Integrity

Students are expected to conduct themselves in accordance with the highest ethical standards of the Profession of Engineering and evince academic integrity in all their pursuits and activities at the university. As such, in accordance with the *General Academic Regulations* on *Academic Integrity*, students are reminded that plagiarism or any other form of cheating in examinations, term tests, assignments, projects, or laboratory reports is subject to serious academic penalty (e.g. suspension or expulsion from the faculty or university). A student found guilty of contributing to cheating by another student is also subject to serious academic penalty.

Accreditation Details

Accreditation Units

- Mathematics: 0%
- Natural Science: 0%
- Complementary Studies: 0%
- Engineering Science: 40%
- Engineering Design: 60%

Graduate Attributes

KB: A knowledge base for engineering
PA: Problem analysis
IN: Investigation
DE: Design
ET: Use of engineering tools
IT: Individual and team work
CS: Communication skills
PR: Professionalism
IE: Impact of engineering on society/ environment
EE: Ethics and equity
EP: Economics and project management
LL: Life-long learning

Competency Levels

1 - Knowledge (Able to recall information)
2 - Comprehension (Ability to rephrase information)
3 - Application (Ability to apply knowledge in a new situation)
4 - Analysis (Able to break problem into its components and establish relationships.)
5 - Synthesis (Able to combine separate elements into a whole)
6 - Evaluation (Able to judge the worth of something)

Grading Scale

Letter	Mark
A+	95–100
A	85–94
B+	80–84
B	70–79
C+	65–69
C	55–64
D	45–54
F	< 45

Note: These boundaries represent a guide for the instructor and class alike. Provided that no individual student is disadvantaged, the instructor may vary any of these boundaries to ensure consistency of grading from year-to-year.

Learning Outcomes

1. Interpret and paraphrase the operation of MOS Transistors and the CMOS Inverter.
2. Design simple logic gates in a bottom up fashion.
3. Evaluate system design and design trade-offs as it pertains to chip level systems.
4. Construct reliability simulations of components and systems.

Expected Competency Levels

Outcome	KB	PA	IN	DE	ET	IT	CS	PR	IE	EE	EP	LL
1	3	3	3	4	6							3
2	4	4	3	3	6							3
3	2	4	3	4	5							3
4	3	5	4	3	6							5

Evaluation

The final course grade is determined by the student's performance on assignments, in laboratories, and on examinations. Students must complete a subset of the laboratories in order to be eligible to receive a passing grade.

Component	Value (%)	Method of Feedback	Learning Outcomes Evaluated
Assignments	5	F, S	1, 2
Laboratories	25	F, S	3, 4
Term Test (Oral)	20	F, S	1, 2, 3
Final Examination	50	S	1, 2, 3

∗ Method of Feedback: **F** - Formative (written comments and/or oral discussion), **S** - summative (numerical grade)

CEAB Graduate Attributes Assessed

PA.4 – Evaluates a solution to a complex engineering problem.

ET.2 – Evaluates and selects appropriate tools for a given scenario.

Requirements and Regulations

- Attendance at lectures and laboratories is important for successful completion of this course. Students must satisfy each evaluation component in the course to receive a final grade.
- It is the responsibility of each student to contact the instructor in a timely manner if he or she is uncertain about his or her standing in the course and about his or her potential for receiving a failing grade. Students should also familiarize themselves with the University's *General Academic Regulations*, as well as Section 3 of the Faculty of Engineering *Academic Regulations* dealing with incomplete term work, deferred examinations, attendance and withdrawal.
- No programmable devices or systems (such as calculators, PDAs, iPods, iPads, cell phones, wireless communication or data storage devices) are allowed in examinations unless approved by the course instructor.
- Students should be aware that they have access to an extensive range of resources and support organizations. These include Academic Resources, Counselling, Advocacy and Accessibility Offices as well as documentation of key University policies e.g. Academic Integrity, Respectful Behaviour, Examinations and related matters.

Supplemental Information

Copyright Notice

Retention of Student Work

Students are advised that copies of their work submitted in completing course requirements (i.e. assignments, laboratory reports, project reports, test papers, examination papers, etc.) may be retained by the instructor and/or the department for the purpose of student assessment and grading, and to support the ongoing accreditation of each Engineering program. This material shall be handled in accordance with the University's *Intellectual Property Policy* and the protection of privacy provisions of *The Freedom of Information and Protection of Privacy Act (Manitoba)*. Students who do not wish to have their work retained must inform the Head of Department, in writing, at their earliest opportunity.